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STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Shannon A. Wichman

Application No./Patent No.: 6,889,318 Filed/Issue Date: 05/03/2005

Entitled: Method for Grouping Non-Interruptible Instructions Prior to Handling an Interrupt Request

VeriSilicon Holdings (Cayman Islands) Co. Ltd. a corporation
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. [✓] the assignee of the entire right, title, and interest; or

2. [ ] an assignee of less than the entire right, title and interest
(The extent (by percentage) of its ownership interest is_____ %)

in the patent application/patent identified above by virtue of either:

A. [✓] An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 018639, Frame 0192, or for which a copy thereof is attached.

OR

B. [ ] A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

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[ ] As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (*i.e.*, a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

_____	January 15, 2007
Signature	Date
David H. Hitt	972-480-8800
Printed or Typed Name	Telephone Number
Attorney for Applicant	
Title	

UNITED STATES PATENT AND TRADEMARK OFFICE

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DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

JANUARY 03, 2007

PTAS

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PLANO, TX 75074

UNITED STATES PATENT AND TRADEMARK OFFICE
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RECORDATION DATE: 11/09/2006

REEL/FRAME: 018639/0192
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BRIEF: SALE

ASSIGNOR:
LSI LOGIC CORPORATION

DOC DATE: 06/30/2006

ASSIGNEE:
VERISILICON HOLDINGS (CAYMAN ISLANDS) CO. LTD.
4699 OLD IRONSIDE DRIVE
SUITE 270
SANTA CLARA, CALIFORNIA 95054

SERIAL NUMBER: 08528509
FILING DATE: 09/12/1995
PATENT NUMBER: 5900025
ISSUE DATE: 05/04/1999
TITLE: PROCESSOR HAVING A HIERARCHICAL CONTROL REGISTER FILE AND METHODS FOR OPERATING THE SAME

SERIAL NUMBER: 08440993 FILING DATE: 05/15/1995
PATENT NUMBER: 5966529 ISSUE DATE: 10/12/1999
TITLE: PROCESSOR HAVING AUXILIARY OPERAND REGISTER FILE AND COMPLEMENTARY ARRANGEMENTS FOR NON-DISRUPTIVELY PERFORMING ADJUNCT EXECUTION

SERIAL NUMBER: 08845817 FILING DATE: 04/29/1997
PATENT NUMBER: 5987603 ISSUE DATE: 11/16/1999
TITLE: APPARATUS AND METHOD FOR REVERSING BITS USING A SHIFTER

SERIAL NUMBER: 08841415 FILING DATE: 04/22/1997
PATENT NUMBER: 5987638 ISSUE DATE: 11/16/1999
TITLE: APPARATUS AND METHOD FOR COMPUTING THE RESULT OF A VITERBI EQUATION IN A SINGLE CYCLE

SERIAL NUMBER: 08401411 FILING DATE: 03/09/1995
PATENT NUMBER: 6081880 ISSUE DATE: 06/27/2000
TITLE: PROCESSOR HAVING A SCALABLE, UNI/MULTI-DIMENSIONAL, AND VIRTUALLY/PHYSICALLY ADDRESSED OPERAND REGISTER FILE

SERIAL NUMBER: 09096409 FILING DATE: 06/11/1998
PATENT NUMBER: 6061876 ISSUE DATE: 05/16/2000
TITLE: TEXTILE RECYCLING MACHINE

SERIAL NUMBER: 09235417 FILING DATE: 01/20/1999
PATENT NUMBER: 6523055 ISSUE DATE: 02/18/2003
TITLE: CIRCUIT AND METHOD FOR MULTIPLYING AND ACCUMULATING THE SUM OF TWO PRODUCTS IN A SINGLE CYCLE

SERIAL NUMBER: 09467939 FILING DATE: 12/21/1999
PATENT NUMBER: 6622154 ISSUE DATE: 09/16/2003
TITLE: ALTERNATE BOOTH PARTIAL PRODUCT GENERATION FOR A HARDWARE MULTIPLIER

SERIAL NUMBER: 09847849 FILING DATE: 04/30/2001
PATENT NUMBER: 6687773 ISSUE DATE: 02/03/2004
TITLE: BRIDGE FOR COUPLING DIGITAL SIGNAL PROCESSOR TO ON-CHIP BUS AS MASTER

SERIAL NUMBER: 09993431 FILING DATE: 11/05/2001
PATENT NUMBER: 6715038 ISSUE DATE: 03/30/2004
TITLE: EFFICIENT MEMORY MANAGEMENT MECHANISM FOR DIGITAL SIGNAL PROCESSOR AND METHOD OF OPERATION THEREOF

SERIAL NUMBER: 09847850 FILING DATE: 04/30/2001
PATENT NUMBER: 6789153 ISSUE DATE: 09/07/2004
TITLE: BRIDGE FOR COUPLING DIGITAL SIGNAL PROCESSOR TO ON-CHIP BUS AS SLAVE

SERIAL NUMBER: 10028898 FILING DATE: 12/20/2001
PATENT NUMBER: 6813704 ISSUE DATE: 11/02/2004
TITLE: CHANGING INSTRUCTION ORDER BY REASSIGNING ONLY TAGS IN ORDER TAG FIELD IN INSTRUCTION QUEUE

SERIAL NUMBER: 10007555 FILING DATE: 11/08/2001
PATENT NUMBER: 6871247 ISSUE DATE: 03/22/2005
TITLE: MECHANISM FOR SUPPORTING SELF-MODIFYING CODE IN A HARVARD ARCHITECTURE DIGITAL SIGNAL PROCESSOR AND METHOD OF OPERATION THEREOF

SERIAL NUMBER: 09924178 FILING DATE: 08/07/2001
PATENT NUMBER: 6889318 ISSUE DATE: 05/03/2005
TITLE: INSTRUCTION FUSION FOR DIGITAL SIGNAL PROCESSOR

SERIAL NUMBER: 10310234 FILING DATE: 12/05/2002
PATENT NUMBER: 6922760 ISSUE DATE: 07/26/2005
TITLE: DISTRIBUTED RESULT SYSTEM FOR HIGH-PERFORMANCE WIDE-ISSUE SUPERSCALAR PROCESSOR

SERIAL NUMBER: 10701775 FILING DATE: 11/05/2003
PATENT NUMBER: 6956788 ISSUE DATE: 10/18/2005
TITLE: ASYNCHRONOUS DATA STRUCTURE FOR STORING DATA GENERATED BY A DSP SYSTEM

SERIAL NUMBER: 09975677 FILING DATE: 10/11/2001
PATENT NUMBER: 6959376 ISSUE DATE: 10/25/2005
TITLE: INTEGRATED CIRCUIT CONTAINING MULTIPLE DIGITAL SIGNAL PROCESSORS

SERIAL NUMBER: 09972404 FILING DATE: 10/05/2001
PATENT NUMBER: 6961844 ISSUE DATE: 11/01/2005
TITLE: SYSTEM AND METHOD FOR EXTRACTING INSTRUCTION BOUNDARIES IN A FETCHED CACHELINE, GIVEN AN ARBITRARY OFFSET WITHIN THE CACHELINE

SERIAL NUMBER: 09901455 FILING DATE: 07/09/2001
PATENT NUMBER: 6963961 ISSUE DATE: 11/08/2005
TITLE: INCREASING DSP EFFICIENCY BY INDEPENDENT ISSUANCE OF STORE ADDRESS AND DATA

SERIAL NUMBER: 10277341 FILING DATE: 10/22/2002
PATENT NUMBER: 6968430 ISSUE DATE: 11/22/2005
TITLE: CIRCUIT AND METHOD FOR IMPROVING INSTRUCTION FETCH TIME FROM A CACHE MEMORY DEVICE

SERIAL NUMBER: 10408387 FILING DATE: 04/07/2003
PATENT NUMBER: 6973630 ISSUE DATE: 12/06/2005
TITLE: SYSTEM AND METHOD FOR REFERENCE-MODELING A PROCESSOR

SERIAL NUMBER: 10047515 FILING DATE: 10/26/2001
PATENT NUMBER: 6976156 ISSUE DATE: 12/13/2005
TITLE: PIPELINE STALL REDUCTION IN WIDE ISSUE PROCESSOR BY PROVIDING MISPREDICT PC QUEUE AND STAGING REGISTERS TO TRACK BRANCH INSTRUCTIONS IN PIPELINE

SERIAL NUMBER: 09993114 FILING DATE: 11/05/2001
PATENT NUMBER: ISSUE DATE:
TITLE: MECHANISM AND METHOD FOR IDENTIFYING AND TRACKING CONDITIONAL INSTRUCTIONS AND DIGITAL SIGNAL PROCESSOR INCORPORATING THE SAME

SERIAL NUMBER: 10002817 FILING DATE: 11/02/2001
PATENT NUMBER: 7013382 ISSUE DATE: 03/14/2006
TITLE: MECHANISM AND METHOD FOR REDUCING PIPELINE STALLS BETWEEN NESTED CALLS AND DIGITAL SIGNAL PROCESSOR INCORPORATING THE SAME

SERIAL NUMBER: 10007498 FILING DATE: 11/13/2001
PATENT NUMBER: ISSUE DATE:
TITLE: PIPELINED MULTIPLY-ACCUMULATE UNIT AND OUT-OF-ORDER COMPLETION LOGIC FOR A SUPERSCALAR DIGITAL SIGNAL PROCESSOR AND METHOD OF OPERATION THEREOF

SERIAL NUMBER: 10066147 FILING DATE: 10/26/2001
PATENT NUMBER: 7107433 ISSUE DATE: 09/12/2006
TITLE: MECHANISM FOR RESOURCE ALLOCATION IN A DIGITAL SIGNAL PROCESSOR BASED ON INSTRUCTION TYPE INFORMATION AND FUNCTIONAL PRIORITY AND METHOD OF OPERATION THEREOF

SERIAL NUMBER: 10066150 FILING DATE: 10/26/2001
PATENT NUMBER: 7085916 ISSUE DATE: 08/01/2006
TITLE: EFFICIENT INSTRUCTION PREFETCH MECHANISM EMPLOYING SELECTIVE VALIDITY OF CACHED INSTRUCTIONS FOR DIGITAL SIGNAL PROCESSOR AND METHOD OF OPERATION THEREOF

SERIAL NUMBER: 10231948 FILING DATE: 08/30/2002
PATENT NUMBER: ISSUE DATE:
TITLE: SYSTEM AND METHOD FOR EXECUTING SOFTWARE PROGRAM INSTRUCTIONS USING A CONDITION SPECIFIED WITHIN A CONDITIONAL EXECUTION INSTRUCTION

SERIAL NUMBER: 10256410 FILING DATE: 09/27/2002
PATENT NUMBER: 7020765 ISSUE DATE: 03/28/2006
TITLE: MARKING QUEUE FOR SIMULTANEOUS EXECUTION OF INSTRUCTIONS IN CODE BLOCK SPECIFIED BY CONDITIONAL EXECUTION INSTRUCTION

SERIAL NUMBER: 10256864 FILING DATE: 09/27/2002
PATENT NUMBER: ISSUE DATE:
TITLE: SYSTEM AND METHOD FOR COOPERATIVE EXECUTION OF MULTIPLE BRANCHING INSTRUCTIONS IN A PROCESSOR

SERIAL NUMBER: 10262414 FILING DATE: 09/30/2002
PATENT NUMBER: ISSUE DATE:
TITLE: SYSTEM AND METHOD FOR EFFICIENT EXECUTION OF LOAD/STORE WITH UPDATE INSTRUCTIONS BY CONDITIONAL UPDATE OF A POINTER

SERIAL NUMBER: 10277339 FILING DATE: 10/22/2002
PATENT NUMBER: 7103757 ISSUE DATE: 09/05/2006
TITLE: SYSTEM, CIRCUIT, AND METHOD FOR ADJUSTING THE PREFETCH INSTRUCTION RATE OF A PREFETCH UNIT

SERIAL NUMBER: 10279344 FILING DATE: 10/24/2002
PATENT NUMBER: ISSUE DATE:
TITLE: IN-CIRCUIT EMULATION DEBUGGER AND METHOD OF OPERATION THEREOF

SERIAL NUMBER: 10299532 FILING DATE: 11/18/2002
PATENT NUMBER: ISSUE DATE:
TITLE: PROCESSOR HAVING A UNIFIED REGISTER FILE WITH MULTIPURPOSE REGISTERS FOR STORING BOTH ADDRESS AND DATA REGISTER VALUES,A PROCESSOR HAVING AN INSTRUCTION DECODER AND AN ASSOCIATED REGISTER MAPPING METHOD

SERIAL NUMBER: 10303610 FILING DATE: 11/25/2002
PATENT NUMBER: ISSUE DATE:
TITLE: METHOD FOR GROUPING NON-INTERRUPTIBLE INSTRUCTIONS PRIOR TO HANDLING AN INTERRUPT REQUEST

SERIAL NUMBER: 10396265 FILING DATE: 03/25/2003
PATENT NUMBER: ISSUE DATE:
TITLE: SYSTEM AND METHOD FOR EVALUATING AND EFFICIENTLY EXECUTING CONDITIONAL INSTRUCTIONS

SERIAL NUMBER: 10420581 FILING DATE: 04/22/2003
PATENT NUMBER: 7028197 ISSUE DATE: 04/11/2006
TITLE: SYSTEM AND METHOD FOR ELECTRICAL POWER MANAGEMENT IN A DATA PROCESSING SYSTEM USING REGISTERS TO REFLECT CURRENT OPERATING CONDITIONS

SERIAL NUMBER: 10437485 FILING DATE: 05/14/2003
PATENT NUMBER: 7079147 ISSUE DATE: 07/18/2006
TITLE: SYSTEM AND METHOD FOR COOPERATIVE OPERATION OF A PROCESSOR AND COPROCESSOR

SERIAL NUMBER: 10603303 FILING DATE: 06/25/2003
PATENT NUMBER: 7051146 ISSUE DATE: 05/23/2006
TITLE: DATA PROCESSING SYSTEMS INCLUDING HIGH PERFORMANCE BUSES AND INTERFACES, AND ASSOCIATED COMMUNICATION METHODS

SERIAL NUMBER: 10613128 FILING DATE: 07/03/2003
PATENT NUMBER: ISSUE DATE:
TITLE: PROCESSOR AND METHOD FOR CONVOLUTIONAL DECODING

SERIAL NUMBER: 10844941 FILING DATE: 05/13/2004
PATENT NUMBER: ISSUE DATE:
TITLE: HARDWARE LOOPING MECHANISM AND METHOD FOR EFFICIENT EXECUTION OF DISCONTINUITY INSTRUCTIONS

SERIAL NUMBER: 11006102 FILING DATE: 12/07/2004
PATENT NUMBER: ISSUE DATE:
TITLE: FOUR ISSUE QUAD LOAD/ STORE MULTIPLY-ACCUMULATE UNIT FOR A DIGITAL SIGNAL PROCESSOR AND METHOD OF OPERATION THEREOF

SERIAL NUMBER: 11081424 FILING DATE: 03/16/2005
PATENT NUMBER: ISSUE DATE:
TITLE: SINGLE-ISSUE DIGITAL SIGNAL PROCESSOR ARCHITECTURE HAVING BACKWARDS-COMPATIBLE INSTRUCTION SET AND METHOD OF OPERATION THEREOF

SERIAL NUMBER: 11083575 FILING DATE: 03/18/2005
PATENT NUMBER: ISSUE DATE:
TITLE: DIGITAL SIGNAL PROCESSOR HAVING INVERSE DISCRETE COSINE TRANSFORM ENGINE FOR VIDEO DECODING AND PARTITIONED DISTRIBUTED ARITHMETIC MULTIPLY/ACCUMULATE UNIT THEREFOR

SERIAL NUMBER: 11083646 FILING DATE: 03/18/2005
PATENT NUMBER: ISSUE DATE:
TITLE: DIGITAL SIGNAL PROCESSOR HAVING INVERSE DISCRETE COSINE TRANSFORM ENGINE FOR VIDEO DECODING AND PARTITIONED DISTRIBUTED ARITHMETIC MULTIPLY/ACCUMULATE UNIT THEREFOR

SERIAL NUMBER: 11128740 FILING DATE: 05/13/2005
PATENT NUMBER: ISSUE DATE:
TITLE: SYSTEM AND METHOD FOR REDUCING THE ADDRESSABLE MEMORY REQUIRED TO EXECUTE A COMPUTER PROGRAM

SERIAL NUMBER: 11222533 FILING DATE: 09/09/2005
PATENT NUMBER: ISSUE DATE:
TITLE: BRANCH PREDICTOR FOR A PROCESSOR AND METHOD OF PREDICTING A CONDITIONAL BRANCH

SERIAL NUMBER: 11246595 FILING DATE: 10/07/2005
PATENT NUMBER: ISSUE DATE:
TITLE: PROCESSOR IMPLEMENTING CONDITIONAL EXECUTION AND INCLUDING A SERIAL QUEUE

SERIAL NUMBER: 11273679 FILING DATE: 11/14/2005
PATENT NUMBER: ISSUE DATE:
TITLE: SYSTEM AND METHOD FOR SIMULTANEOUSLY EXECUTING MULTIPLE CONDITIONAL EXECUTION INSTRUCTION GROUPS

MARY BENTON, EXAMINER
ASSIGNMENT SERVICES BRANCH
PUBLIC RECORDS DIVISION

NOV. 9. 2006 9:57AM HITT GAINES 9724808865 NO. 6889 P. 2

11-13-2006

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To the Director of the U.S. Patent and Trademark Office: Please record the attached documents or the new address(es) below.

1. Name of conveying party(ies)

LSI Logic Corporation
1621 Barber Lane
M/S D-106
Milpitas, CA 95035

Additional name(s) of conveying party(ies) attached? [x] Yes [ ] No

2. Name and address of receiving party(ies)

Name: VeriSilicon Holdings (Cayman Islands) Co. Ltd.

Internal Address: Suite 270

Street Address: 4699 Old Ironside Drive,

City: Santa Clara

State: California

Country: USA Zip: 95054

Additional name(s) & address(es) attached? [ ] Yes [x] No

3. Nature of conveyance/Execution Date(s):

Execution Date(s) June 30, 2006

- [ ] Assignment
- [ ] Merger
- [ ] Security Agreement
- [ ] Change of Name
- [ ] Joint Research Agreement
- [ ] Government Interest Assignment
- [ ] Executive Order 9424, Confirmatory License
- [x] Other Sale

4. Application or patent number(s): [ ] This document is being filed together with a new application.

A. Patent Application No.(s)

B. Patent No.(s)

Additional numbers attached? [x] Yes [ ] No

5. Name and address to whom correspondence concerning document should be mailed:

Name: Prasad Kalluri

Internal Address: Suite 430

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City: Plano

State: Texas Zip: 75074

Phone Number: 972-244-5130

Fax Number: 972-244-5101

Email Address: prasad.kalluri@verisilicon.com

6. Total number of applications and patents involved:

7. Total fee (37 CFR 1.21(h) & 3.41) $ 2,080.00

- [ ] Authorized to be charged by credit card
- [x] Authorized to be charged to deposit account
- [ ] Enclosed
- [ ] None required (government interest not affecting title)

8. Payment Information

a. Credit Card Last 4 Numbers
Expiration Date

b. Deposit Account Number 08-2395

Authorized User Name David H. Hitt

9. Signature: [signature]
Signature

Nov 8, 2006
Date

SESHAGIRI PRASAD KALLURI
Name of Person Signing

Total number of pages including cover sheet, attachments, and documents: 8

Documents to be recorded (including cover sheet) should be faxed to (571) 273-0140, or mailed to:
Mail Stop Assignment Recordation Services, Director of the USPTO, P.O. Box 1450, Alexandria, V.A. 22313-1450

Patents and Patent Applications

Issued Patents

No.	Serial No.	Issue No.	Patent Title	Filing Date	Issue Date
1	08/528,509	5,900,025	A processor having a hierarchical control register file and methods for operating the same	9/12/1995	5/4/1999
2	08/440,993	5,956,529	Auxiliary operand register file and complementary arrangements for non-disruptively performing adjunct execution by a processor having a virtually addressable primary operand register file	5/15/1995	10/12/1999
3	08/845,817	5,987,605	An apparatus and method for reversing bits using a shifter	4/28/1997	11/16/1999
4	08/841,415	5,987,638	An Apparatus and method for computing the results of a viterbi equation in a single cycle	4/22/1997	11/16/1999
5	09/401,411	6,081,880	Processor having a scalable unimultidimensional and virtually/physically addresses operand register file	9/9/1995	6/27/2000
6	09/099,403	6,260,112	Register Memory Linking	3/5/1998	7/10/2001
7	09/295,417	6,523,055	Circuit and method for multiplying and accumulating the sum of two products in a single cycle	1/20/1999	2/18/2003
8	09/467,939	6,622,154	Alternate Booth Partial Product Generation for a Hardware Multiplier	12/21/1999	9/16/2003
9	09/847,849	6,687,773	Bridge For Coupling Digital signal Processor To On-Chip Bus As Master	4/30/2001	2/3/2004
10	09/993,431	6,715,038	Efficient Memory Management Mechanism for Digital Signal Processor and Method of Operation Thereof	11/5/2001	3/30/2004
11	09/847,850	6,769,153	Using AMBA For Signal Processor Core Integration	4/30/2001	9/7/2004
12	10/028,898	6,813,704	Changing Instruction Order By Reassigning Only Tags In Order Tag Field In Instruction Queue	12/20/2001	11/2/2004
13	10/007,555	6,871,247	A Method For Memory Sharing And Self-Modifying Code Handling In A Harvard Architecture DSP	11/8/2001	3/22/2005
14	09/924,178	6,889,316	Instruction Fusion For Digital Signal Processor	8/7/2001	5/3/2005
15	10/310,234	6,922,760	Distributed Result System for High-Performance Wide-Issue Superscalar Processor	12/5/2002	7/26/2005
16	10/701,775	6,956,766	Asynchronous Data Structure for Storing Data Generated by a DSP System	11/5/2003	10/18/2005
17	09/975,677	6,959,376	Integrated Circuit Containing Multiple Digital Signal Processors	10/11/2001	10/25/2005

No.	Serial No.	Issue No.	Patent Title	Filing Date	Issue Date
18	09/972,404	6,961,844	System and Method for Extracting Instruction Boundaries in a Fetched Cache line, Given an Arbitrary Offset within the Cache line	10/5/2001	11/1/2005
19	09/901,455	6,963,961	Increasing DSP Efficiency by Independent Issuance of Store Adress and Data	7/5/2001	11/8/2005
20	10/277,341	6,968,430	Circuit and Method for Improving Instruction Fetch Time from a Cache Memory Device	10/22/2002	11/22/2005
21	10/405,387	6,978,330	System and Method for Reference-Modeling a Processor	4/7/2003	12/6/2005
22	10/047,515	6,976,155	Pipeline Stall Reduction in Wide Issue Processor by Providing Mispredict PC Queue and Staging Registers to Track Branch Instructions in Pipeline	10/26/2001	12/13/2005

Patent Applications

No.	Serial No.	Issue No.	Patent Title	Filing Date	Issue Date
1	09/993,114		Mechanism and Method For Conditionally Executing Instructions and Digital Signal Processor Incorporating The Same	11/5/2001	
2	10/002,617	7,013,382	Mechanism And Method For Reducing Pipeline Stalls Between Nested Calls and Digital Signal Processor Incorporating The Same	11/2/2001	3/14/2006
3	10/007,498		Pipelined Multiply-Accumulate Unit and Out-Of-Order Completion Logic For A Superscalar Digital Signal Processor And Method Of Operation Thereof	11/13/2001	
4	10/056,147		Mechanism for Resource Allocation in a Digital Signal Processor and Method of Operation Thereof	10/26/2001	
5	10/056,150		A Method For Instruction Prefetch In A Four-Way Superscalar Harvard Architecture DSP With A Small Direct-Mapped Instruction Cache	10/26/2001	
6	10/231,945		System and Method for Conditionally Executing Software Program Instructions	8/30/2002	
7	10/256,410	7,020,765	System and Method for Simultaneously Executing Multiple Conditional Execution Instruction Groups	9/27/2002	3/28/2006
8	10/255,854		System And Method For Conditionally Executing An Instruction Dependent On A Previously Existing Condition	9/27/2002	
9	10/262,414		System and Method For Selectively Updating Pointers Used in Conditionally Executed Load/Store With Update Instructions	9/30/2002	

No.	Serial No.	Issue No.	Patent Title	Filing Date	Issue Date
10	10/277,398		System, Circuit, and Method for Adjusting Prefetch Instruction Rate	10/22/2002	
11	10/279,844		In-Circuit Emulation Debugger and Method of Operation Thereof	10/24/2002	
12	10/299,532		Processor Having a Unified Register File with Multipurpose Registers for Storing Address and Data Register Values, and Associated Register Mapping Method	11/18/2002	
13	10/303,610		Method for Grouping Non-Interruptible Instructions Prior to Handling an Interrupt Request	11/25/2002	
14	10/396,265		System and Method for Evaluating and Efficiently Executing Conditional Instructions	3/25/2003	
15	10/420,581	7,028,197	System and Method For Electrical Power Management in a Data Processing System Using Registers To Reflect Current Operating Conditions	4/22/2003	4/11/2006
16	10/437,485		System and Method For Cooperative Operation Of A Processor And Coprocessor	5/14/2003	
17	10/603,309	7,051,145	Data Processing Systems Including High-Performance Buses and Interfaces, and Associated Communication Methods	6/25/2003	5/23/2006
18	10/613,128		Processor and Method for Convolutional Decoding Hardware Looping Mechanism and	7/3/2003	
19	10/844,941		Method for Efficient Execution of Discontinuity Instructions	5/13/2004	
20	11/008,102		Four Issue Quad Load/Store Multiply-Accumulate Unit for a Digital Signal Processor and Method of Operation Thereof	12/7/2004	
21	11/081,424		Single-Issue Digital Signal Processor Architecture Having Backwards-Compatible Instruction Set and Method of Operation Thereof	3/16/2005	
22	11/083,575		DIGITAL SIGNAL PROCESSOR HAVING INVERSE DISCRETE COSINE TRANSFORM ENGINE FOR VIDEO DECODING AND PARTITIONED DISTRIBUTED ARITHMETIC MULTIPLY/ACCUMULATE UNIT THEREFOR	3/18/2005	
23	11/083,646		DIGITAL SIGNAL PROCESSOR HAVING INVERSE DISCRETE COSINE TRANSFORM ENGINE FOR VIDEO DECODING AND PARTITIONEDDISTRIBUTED ARITHMETIC MULTIPLY/ACCUMULATE UNIT THEREFOR	3/18/2005	

No.	Serial No.	Issue No.	Patent Title	Filing Date	Issue Date
24	11/128,740		System and Method for Reducing the Addressable Memory Required to Execute a Computer Program	5/13/2005	
25	11/222,535		Branch Predictor For A Processor And Method Of Predicting A Conditional Branch	9/9/2005	
26	11/246,595		Processor Implementing Conditional Execution and Including a Serial Queue	10/7/2005	
27	11/273,679		System and Method for Simultaneously Executing Multiple Conditional Execution Instruction Groups	11/14/2005	
28	LSI Docket # 05-1230		Floating point data format for fast execution on fixed point processors		
29	LSI Docket # 05-1690		A Processor Independent Cache Management Mechanism		
30	LSI Docket # 05-2212		Floating Point Hardware Accelerator-Coprocessor for Fixed-Point Processors based on the ZSP Fast Floating Point Format (ZSPFF)		

ASSIGNMENT OF PATENT

For good and valuable consideration, the receipt of which is hereby acknowledged, each of LSI LOGIC CORPORATION, a Delaware corporation ("LSILogic"), having offices at 1621 Barber Lane, Milpitas, CA 95035, and LSI LOGIC HK HOLDINGS, an exempted company with limited liability under the laws of Cayman Islands and a wholly-owned subsidiary of LSI Logic Corporation (together with LSI Logic, the "Assignors"), the mailing address of which is PO Box 10344T, Harbour Place, 4th Floor, 103 South Church Street, Grand Cayman, Cayman Islands, does hereby sell, assign and transfer and agrees to sell, assign and transfer unto VERISILICON HOLDINGS (CAYMAN ISLANDS) CO., LTD., an exempted company with limited liability under the laws of the Cayman Islands ("Assignee"), having offices at 4699 Old Ironsides Drive, Suite 270, Santa Clara, CA 95054, or its designee, all of such Assignor's right, title and interest in and to the following Patent Applications, Letters Patent and any reissues and continuations thereof:

U.S. Patent or Application No.	Issue Date Filing Date Inventor	Description

and in all counterparts of the foregoing patents filed or issued in foreign countries, as to which such Assignor agrees to furnish and to execute on a country-by-country basis specific Assignments as requested by Assignee or any such designee.

Each of the Assignors covenants that it is the sole owner and assignee and holder of record title to the above-identified United States Letters Patent (and foreign counterparts thereto), as applicable, by virtue of assignments as to the U.S. filed patents and applications previously executed and recorded in the United States Patent and Trademark Office and that it has full power to make the present assignment.

Each of the Assignors further sells, assigns, transfers and conveys on to Assignee the entire right, title and interest in and to any and all causes of action and rights or recovery for past infringement of the applicable Letters Patent herein assigned.

Each of the Assignors also hereby authorizes, as applicable, the Commissioner of Patents to issue any and all Letters Patent which may be granted upon any of the patent applications herein referenced to Assignee, as the assignee to the entire interest thereto.

LSI LOGIC CORPORATION

By: _____

Title: _____

LSI LOGIC HK HOLDINGS

By: _____

Title: _____

ATTEST:

By: _____

Title: _____

LSI LOGIC CORPORATION

By: Bryon Look

Title: EVP & CFO

LSI LOGIC HK HOLDINGS

By: Bryon Look

Title: President and Director

ATTEST:

By: Becky A. Abella

Title: Executive Assistant

CERTIFICATION

STATE OF California)
) ss.
COUNTY OF Santa Clara)

On this 30 day of June 2006, before me, the undersigned, a Notary Public for the State of California, personally appeared Bryan Lane, personally known to me (or proved to me on the basis of satisfactory evidence) to be the person who executed the foregoing instrument as Vice President of the corporation named therein, and acknowledged to me that he executed the same as his voluntary act on behalf of such corporation with authority to do so for the purposes therein set forth.

Becky A. Abella
Notary Public

My Commission expires: Aug 15, 2009

BECKY A. ABELLA
Commission # 1599921
Notary Public - California
Santa Clara County
My Comm. Expires Aug 15, 2009

Assignment of Patent